REMARKS

In response to the Final Action of 01/11/2007, the applicant has filed Request for Continued Examination (RCE). Prior to the continued examination, new claims have been filed to capture proper scope of the invention.

On page 2 of the Action, claims 44 to 52 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Chittipeddi et al.* (US 6,556,409), in view of Applicant's admitted prior art.

The applicants respectfully traverse the rejections under 35 U.S.C. 103(a) and request reconsideration. Claims 44 to 52 are not unpatentable over *Chittipeddi et al.* (US 6,556,409), in view of the Applicant's admitted prior art, for the reasons explained below.

As recited in claim 44, a semiconductor device of the invention comprises: a semiconductor chip including an inner circuit, an input pad, and a wiring for connecting the input pad to the inner circuit; a plurality of electrostatic protection elements connected to the wiring between the input pad and the inner circuit; and a fuse disposed between the wiring and at least one of the electrostatic protection elements.

In particular, the semiconductor device of the invention has a plurality of the electrostatic protection elements connected to the wiring between the input pad and the inner circuit. Further, the fuse is disposed between the wiring and at least one of the electrostatic protection elements. Accordingly, it is possible to easily adjust a capacity of the semiconductor device, which is a sum of capacities of the electrostatic protection elements.

On page 2 of the Final Action, the examiner states "each single FET which makes up part of an ESD protection component can be considered as an individual element. That is, the prior art structure shown in FIG. 14 can be considered to contain two separate elements, namely the p channel FET and the n channel FET."

However, according to the definition the applicant has used consistently throughout the whole specification, the examiner's above statement is not correct.

In the specification, there is a description of "The electrostatic protection element 1 is a capacitor of CMOS transistors in which a P-channel MOS transistor Pch and an N-channel MOS transistor Nch are connected to each other." (page 2, lines 2 to 5 of the specification)

As clearly defined in the description, the electrostatic protection element is formed of the p channel transistor and the n channel transistor. Therefore, the p channel transistor and the n channel transistor are not equivalent to the electrostatic protection element. Therefore, each single FET which makes up part of an ESD protection component cannot be considered as an individual element. This definition has been used consistently throughout the whole specification, including claims.

As explained above, the Applicant's admitted prior art does not disclose the semiconductor device of the invention having a plurality of the electrostatic protection elements connected to the wiring between the input pad and the inner circuit.

Chittipeddi et al. has disclosed an integrated circuit. In Fig. 1a in *Chittipeddi et al.*, two integrated circuits 5 and 10 are coupled together via input and output (I/O) circuitry 20 to form a multi-chip module. Each of the integrated circuits 5 and 10 includes I/O circuitries 15 and 20 having electrostatic discharge (ESD) protection components (col. 3, lines 44-51). As shown in Fig. 1b in *Chittipeddi et al.*, the I/O circuitry 20 includes an I/O buffer 100 coupled to a bond pad 105 (col. 4, lines 12-14). The I/O circuitry 20 may further include an ESD protection component 115 coupled to the bond pad 105 via an enable/disable component 110. The enable/disable component 110 may be a fusible link that provides an electrical interconnection between the bond pad 105 and the ESD protection component 115 (col. 4, lines 24-31). Further, as shown in Fig. 1c, the I/O circuitry 15 includes an I/O buffer 130 coupled to a bond pad 135, and the bond pad 135 is coupled to an ESD protection component 140. However, the I/O circuitry 15 does not include the enable/disable component 110.

In the invention recited in claim 44, the semiconductor device has a plurality of the electrostatic protection elements, and the electrostatic protection elements are connected to the wiring between the input pad and the inner circuit. Further, the fuse is disposed between the wiring and at least one of the electrostatic protection elements. Accordingly, through disconnection of the fuse, it is possible to adjust a capacity of the semiconductor device, which is a sum of capacities of the electrostatic protection elements.

Chittipeddi et al. has disclosed two types of I/O circuitries

15 and 20. However, both of the I/O circuitries 15 and 20 have the single ESD protection component 115 or 140. Accordingly, each of the I/O circuitries 15 and 20 has a constant capacity corresponding that of the single ESD protection component 115 or 140, and it is not possible to adjust a capacity of the semiconductor. In *Chittipeddi et al.*, there is no disclosure or suggestion regarding the semiconductor device having a plurality of the electrostatic protection elements.

Claim 1 of *Chittipeddi et al.* states as follows:

1. A device comprising:

a first electrostatic discharge (ESD) protection circuit configured to protect a first input/output circuit of said device, wherein said first input/output circuit is configured to couple said device to a second device;

a second ESD protection circuit configured to protect a second input/output circuit of said device; and

circuitry adapted to selectively enable and disable said first ESD protection circuit.

As recited claim 1 of *Chittipeddi et al.*, the first electrostatic discharge (ESD) protection circuit protects the first input/output circuit, and the second ESD protection circuit protects the second input/output circuit. As obvious from the description, the ESD protection circuit is connected to the first input/output circuit, and the second ESD protection circuit is connected to the second input/output circuit. The description does not disclose or suggest a plurality of the electrostatic protection elements connected to one single input/output circuit. In *Chittipeddi et al.*, there is no disclosure or suggestion regarding the semiconductor device having a plurality of the

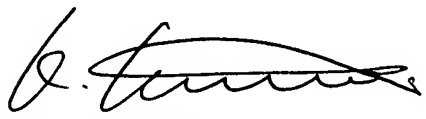
electrostatic protection elements.

As explained above, the cited references do not disclose nor suggest all the features of the invention recited in claim 44. Even through the cited references are combined, without any concrete motivation supported by a clear evidence, the invention recited in claim 44 is not obvious.

Reconsideration and allowance are earnestly solicited.

Three-month extension of time has been requested. The credit card payment form in the amount of $1,810 (three-month extension fee $1,020, RCE $790) has been attached herewith.

Respectfully submitted,



Kazunao Kubotera
Reg. No. 51,194

TAKEUCHI & KUBOTERA, LLP
200 Daingerfield Rd.
Suite 202
Alexandria, VA 22314
Tel. (703) 684-9777